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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/741,845	12/22/2000	Richard P. Modelski	P 270191 NOR-13183BA	8543

34845 7590 07/08/2005

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EXAMINER	
ZHEN, LI B	

ART UNIT	PAPER NUMBER
2194	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/741,845	MODELSKI ET AL.	
	Examiner	Art Unit	
	Li B. Zhen	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 16 and 18 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed September 23, 2004 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language [Foreign reference DE3111991A1]. It has been placed in the application file, but the information referred to therein has not been considered.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 1 – 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent NO. 6,625,654 to Wolrich et al. [hereinafter referred**

to as Wolrich, cited in the previous office action] in view of U.S. Patent NO. 6,606,704 to Adiletta et al. [hereinafter referred to as Adiletta].

6. As to claim 1, Wolrich teaches the invention substantially as claimed including a method for sharing at least one computer resource [shared resource] between a plurality of instruction threads [program threads] of a multi-threaded process [program threads also communicate with a shared resource; col. 11, lines 10 – 21], the method comprising:

providing a processor including [hardware-based multithreaded processor 12, Fig. 1; col. 1, line 57 – col. 2, line 25] a plurality of analysis machines [hardware-based multithreaded processor 12 has multiple microengines 22, Fig. 1; col. 2, lines 1 – 5] and a plurality of computer resources [microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and 28, Fig. 1; col. 2, lines 32 – 46];

executing each instruction thread [program threads] in one of the plurality of analysis machines [multiple microengines 22 each with multiple hardware controlled program threads that can be simultaneously active and independently work on a task; col. 1, line 57 – col. 2, line 25]; and

sharing services of at least one of the plurality of computer resources [shared resources including memory system 16 and bus interface 24 and 28] between at least two of the plurality of analysis [microengines] machines [six microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and

28; col. 2, lines 32 – 47] during the execution of each instruction thread [program threads could request the same shared resource; col. 2, lines 46 – 60].

7. Although Wolrich teaches the invention substantially, Wolrich does not specifically teaches that each of the plurality of analysis machines include an internal pipeline and is communicably coupled to a plurality of shared pipelines.

However, Adiletta teaches a processor [parallel, hardware-based multithreaded processor 12, Fig. 1; col. 2, lines 55 – 67] including a plurality of analysis machines [hardware-based multithreaded processor 12 has multiple microengines 22, Fig. 1; col. 2, lines 55 – 67] and a plurality of computer resources [microengines 22a-22f operate with shared resources including memory system 16; col. 3, lines 28 – 42] wherein each of the plurality of analysis machines includes an internal pipeline [microengine datapath maintains a 5-stage micro-pipeline 82; col. 8, lines 28 – 37] and is communicably coupled to a plurality of shared pipelines [SRAM controller 26b performs memory reference sorting to minimize delays (bubbles) in the pipeline from the SRAM interface 140 to memory 16b; col. 18, lines 56 – 62; col. 3, line 50 – col. 4, line 12].

8. It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply the teaching of a plurality of analysis machines that include an internal pipeline and is communicably coupled to a plurality of shared pipelines as taught by Adiletta to the invention of Wolrich because the pipeline provides lookup of microinstruction words, formation of register file addresses, read of operands from register file, ALU, shift or compare operations, and write-back of results to registers, which allows simultaneous register file read and write [col. 8, lines 29 - 37 of Adiletta].

9. As to claim 2, Wolrich teaches, transferring data from an input buffer [FBUS interface 28 provides the ability to input large amounts of data using a series of input and output FIFO's 29a-29b; col. 4, lines 18 – 31] to a packet task manager [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18];

dispatching the data from the packet task manager to one of the plurality of analysis machines [From the FIFOs 29a-29b, the microengines 22a-22f fetch data from...a receive FIFO in which data has come from a device on bus 18, into the FBUS interface 28...Data functions are distributed amongst the microengines; col. 4, lines 17 – 48];

classifying the data in the one analysis machine [microengines pass the packets off for more detailed processing such as in boundary conditions; col. 2, lines 5 – 23];

modifying and forwarding the data in a packet manipulator [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30].

10. As to claim 3, Wolrich teaches transferring the data [interface 28 includes a push state machine 200 for pushing data into the transfer registers; col. 8, lines 37 – 50] after modifying and forwarding to an output buffer [FBI 28 contains a Transmit FIFO 182; col. 8, lines 37 – 50].

11. As to claim 4, Wolrich teaches, processing data at a rate of at least 10 Gbs [a router, the hardware-based multithreaded processor 12 interfaces to network devices such as a media access controller device...a Gigabit Ethernet device 13b; col. 2, lines 57 – 67].

12. As to claim 5, Wolrich as modified teaches an apparatus for sharing at least one computer resource [shared resource of Wolrich] between a plurality of instruction threads [program threads of Wolrich] of a multi-threaded process [program threads also communicate with a shared resource; col. 11, lines 10 – 21 of Wolrich], the apparatus comprising:

a plurality of analysis machines [hardware-based multithreaded processor 12 has multiple microengines 22, Fig. 1; col. 2, lines 1 – 5 of Wolrich] to execute a plurality of instruction threads [multiple microengines 22 each with multiple hardware controlled program threads that can be simultaneously active and independently work on a task; col. 1, line 57 – col. 2, line 25 of Wolrich], wherein each of said plurality of analysis machines includes an internal pipeline [microengine datapath maintains a 5-stage micro-pipeline 82; col. 8, lines 28 – 37 of Adiletta] and is communicably coupled to a plurality of shared pipelines [SRAM controller 26b performs memory reference sorting to minimize delays (bubbles) in the pipeline from the SRAM interface 140 to memory 16b; col. 18, lines 56 – 62; col. 3, line 50 – col. 4, line 12 of Adiletta];

a plurality of computer resources [microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and 28, Fig. 1; col. 2,

lines 32 – 46 of Wolrich] operationally connected to the plurality of analysis machines [hardware-based multithreaded processor 12 has multiple microengines 22, Fig. 1; col. 2, lines 1 – 5 of Wolrich];

wherein each instruction thread [program threads of Wolrich] executes in one of the plurality of analysis machines [multiple microengines 22 each with multiple hardware controlled program threads that can be simultaneously active and independently work on a task; col. 1, line 57 – col. 2, line 25 of Wolrich], and services of at least one of the plurality of computer resources are shared [shared resources including memory system 16 and bus interface 24 and 28 of Wolrich] between at least two of the plurality of analysis [microengines of Wolrich] machines [six microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and 28; col. 2, lines 32 – 47 of Wolrich] during the execution of each instruction thread [program threads could request the same shared resource; col. 2, lines 46 – 60 of Wolrich].

13. As to claim 6, Wolrich teaches packet task manager operationally connected [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18] to the analysis machines [From the FIFOs 29a-29b, the microengines 22a-22f fetch data; col. 4, lines 17 – 48], and packet manipulator operationally connected to the analysis machines [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30].

14. As to claim 7, Wolrich teaches sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process [microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and 28, Fig. 1; col. 2, lines 32 – 46], wherein the analysis machines are multi-threaded [multiple microengines 22 each with multiple hardware controlled program threads that can be simultaneously active and independently work on a task; col. 1, line 57 – col. 2, line 25].

15. As to claim 8, Wolrich teaches sharing at least one computer resource between a plurality of instruction threads of a multi-threaded process [microengines 22a-22f operate with shared resources including memory system 16 and bus interfaces 24 and 28, Fig. 1; col. 2, lines 32 – 46], wherein the analysis machines each have 32 threads [multiple microengines 22 each with multiple hardware controlled program threads that can be simultaneously active and independently work on a task; col. 1, line 57 – col. 2, line 25].

16. As to claim 10, Wolrich teaches an external memory engine [Transmit FIFO 182, a Receive FIFO 183] operationally connected to the analysis machines [multiple microengines 22; col. 1, line 57 – col. 2, line 25], and a hash engine operationally connected to the analysis machines [FBI 28 contains a Transmit FIFO 182, a Receive FIFO 183, a HASH unit 188; col. 8, lines 35 – 50].

17. **Claims 9 and 11 – 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolrich and Adiletta further in view of U.S. Patent NO. 6,081,860 to Bridges [cited in previous office action].**

18. As to claim 9, Wolrich as modified teaches the invention substantially as claimed including a packet task manager operationally [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18 of Wolrich] connected to the analysis machines [From the FIFOs 29a-29b, the microengines 22a-22f fetch data; col. 4, lines 17 – 48 of Wolrich], a packet manipulator operationally connected to the analysis machines [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30 of Wolrich], and a global access bus [FBUS interface 28 is responsible for controlling and interfacing the processor 12 to the FBUS 18; col. 3, lines 2 – 15 of Wolrich].

19. Although Wolrich as modified teaches the invention substantially, Wolrich as modified does not teaches a master request bus and a slave request bus separated form each other and pipelined.

However, Bridges teaches enabling a device to accomplish address pipelining for both read and write operation between master and slave devices on a processor local bus [col. 2, lines 45 – 67], a master request bus [Each master 20 and 22 also has corresponding address busses (M0ABus and M1ABus), write data busses (M0WrDBus and M1WrDBus), read data busses (M0RdDBus and M1RdDBus) and transfer qualifier

signal busses (M0TQuals and M1TQuals) connecting the respective master devices M0 and M1 to the arbiter device 24; col. 4, lines 23 – 49] and a slave request bus separated form each other and pipelined [slave devices 26 and 28 are also connected to each other and to the arbiter device 24 by a write data bus (WrDBus) and also a separate read data bus (RdDBus); col. 4, lines 49 – 67].

20. It would have been obvious to a person of ordinary skill in the art at the time of the invention to apply the teaching of a master request bus and a slave request bus separated form each other and pipelined as taught by Bridges to the invention of Wolrich as modified because this allows for the overlapping of read and write data transfers and provides high bandwidth data transfers by performing read and write data transfers simultaneously [col. 1, lines 37 – 45 of Bridges].

21. As to claim 11, Wolrich as modified teaches packet input global access bus software code [FBUS interface 28] used for flow of data packet information from a flexible input data buffer to an analysis machine [FBUS interface 28 provides the ability to input large amounts of data using a series of input and output FIFO's 29a-29b. From the FIFOs 29a-29b, the microengines 22a-22f fetch data; col. 4, lines 15 – 30 of Wolrich].

22. As to claims 12 and 15, Wolrich as modified teaches packet data global [shared bus; col. 4, line 13 – 15 of Wolrich] access bus software code used for flow of packet data [interface 28 also includes a controller 28a that performs header processing of

incoming packets from the FBUS 18; col. 4, lines 1 – 18 of Wolrich] between a flexible data input bus and a packet manipulator [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30 of Wolrich].

23. As to claim 13, Wolrich as modified teaches statistics data global access bus [FBUS unit (via Mbus); col. 4, lines 13 – 15 of Wolrich] software code used for connection [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18 of Wolrich] of an analysis machine to a packet manipulator [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30 of Wolrich].

24. As to claim 14, Wolrich as modified teaches private data [FBUS unit (via private bus); col. 4, line 13 – 15 of Wolrich] global access bus software code [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18 of Wolrich] used for connection of an analysis machine to an internal memory engine submodule [controller 28a extracts the packet headers and performs a microprogrammable. source/destination/protocol hashed lookup; col. 4, lines 1 – 30 of Wolrich].

25. As to claim 16, Wolrich as modified teaches results global access bus software code used for providing [interface 28 also includes a controller 28a that performs header processing of incoming packets from the FBUS 18; col. 4, lines 1 – 18 of Wolrich], flexible access to an external memory [sum of the bandwidths of the internal buses in the processor 12 exceed the bandwidth of external buses coupled to the processor 12; col. 3, lines 13 – 31 of Wolrich].

26. As to claim 18, Wolrich as modified teaches a bi-directional access port operationally connected to the analysis machine [FBI interface 28 that specifies a port from which to extract the data and the Receive FIFO element to use to buffer that data as well as the microengine context to be notified once the receive data has been fetched; col. 10, lines 55 – 62 of Wolrich], and a flexible data input [Receive FIFO] and output buffer [Transmit FIFO] operationally connected to the analysis machine machines [FBI 28 contains a Transmit FIFO 182, a Receive FIFO 183, a HASH unit 188; col. 8, lines 35 – 50 of Wolrich].

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,532,509 to Wolrich et al. teaches a parallel, multi-threaded processor system and technique for arbitrating command requests.

U.S. Patent No. 6,661,794 to Wolrich et al. teaches a network processor that has multiple processing elements, each processing element supporting multiple simultaneous program threads with access to shared resources in an interface.

U.S. Patent No. 6,668,317 to Bernstein et al. teaches a parallel hardware-based multithreaded processor.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen
Examiner
Art Unit 2194

lbz

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